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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P5567
First Inventor or Application Identifier	Vincent E. Hummel
Title	BRANCH PREDICTOR WITH SATURATING COUNTER AND LOCAL BRANCH
Express Mail Label No.	EM014065505US

JC639 U.S. PTO 03/28/00

jc675 U.S. PTO 09/535765 03/28/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form *(e.g. PTO/SB/17)*
(Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* 21
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C.113)* *Total Sheets* 4
4. Oath or Declaration *Total Pages*
   a. [X] Newly executed (original copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 16 completed)
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

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5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
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ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO - 1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
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13. [ ] *Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
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Prior application Information: Examiner ____ *Group/Art Unit:* ____

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Attorney's Docket No. 042390.P5567
Express Mail No. EM014065505US

UNITED STATES PATENT APPLICATION

FOR

BRANCH PREDICTOR WITH SATURATING COUNTER AND LOCAL BRANCH HISTORY TABLE

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BRANCH PREDICTOR WITH SATURATING COUNTER AND LOCAL BRANCH HISTORY TABLE

Field of the Invention

This invention is generally related to pipelined processors and more particularly to branch prediction methodologies implemented in such processors.

Background

Advanced processors use pipelining techniques to execute instructions at very high speeds. A pipeline is like an assembly line. In an automobile assembly line, there are many steps, each contributing to the construction of the car. Each step operates in parallel with the other steps, though on a different car. In a processor pipeline, each step completes a part of an instruction. Like the assembly line, different steps are completing different parts of different instructions in parallel. Each of these steps is called a pipe stage. The stages are connected one to the next to form a pipe where instructions enter at one end, progress through the stages, and exit at the other end. A pipeline is most effective if it can process a steady stream of instructions in a sequential manner.

When a branch is executed, it may change the instruction pointer (IP) to something other than its current value plus a predetermined fixed increment. If a branch changes the IP to the address of the branch target (given by the branch instruction), it is a "taken" branch. If it falls through, it is "not taken". Knowledge of whether the branch will be taken or not, and the address of the branch target, typically becomes available when the instruction has reached the last or next to last stage of the pipe. This means that all instructions that issued later than the branch- and hence not as far along in the pipe as the branch- are invalid, i.e. they should not be executed, if the branch is taken, because the next instruction to be executed following the branch is

the one at the target address. All of the time spent by the pipeline on the later issued instructions is wasted delay, thus significantly reducing the speed improvement that can be obtained from the pipeline. To alleviate the delay that may be caused by the branch, there are two steps that can be taken. First, find out whether the branch will be taken or not taken (the "direction" of the branch) earlier in the pipeline. Second, compute the target address earlier.

One method for dealing with branches is to use hardware inside the processor to predict whether an address will result in a branch instruction being taken or not taken. Examples of such hardware include the 2-bit saturating counter predictor (see "Computer Architecture A Quantitative Approach", David A. Patterson and John L. Hennessy, 2d Edition, Morgan Kauffman Publishers, pp. 262-271,) and the local history predictor which uses the past behavior (taken/not-taken) of a particular branch instruction to predict future behavior of the instruction. The use of a combination of two different predictors has been proposed to obtain more accurate predictions, where in U.S. patent no. 5,758,142 the final prediction at the output of a multiplexer is selected between a prediction provided using a branch past history table and one provided using a global branch history table, where the selection is made according to the most significant bit of a counter. Another technique uses the combination of the local history predictor and the saturating counter predictor to achieve more accurate predictions than either one can by itself, by using the branch history (obtained from a matching entry in a local history table) to index into a pattern history table, where the next execution of a branch is finally predicted by the value of a 2-bit saturating counter predictor. See article by T. Yeh and Y. N. Patt, "Alternative Implementations of Two-Level Adaptive Branch Prediction", Proc. 19th Symposium on Computer Architecture

(May 1992) Gold Coast, Australia 124-134. Implementation of both of these techniques, however, requires a relatively large area on the processor chip.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated by way of example and not by way of limitation in the figures of the accompanying drawings in which like references indicate similar elements and in which:

Fig. 1 illustrates a block diagram of branch prediction logic according to an embodiment of the invention.

Fig. 2 shows a state diagram of a saturating counter branch predictor.

Fig. 3 illustrates the relationship between an address, the instructions to which the address points, and the generation of an index and tag value.

Fig. 4 is a block diagram of part of a pipelined processor featuring branch direction prediction logic.

DETAILED DESCRIPTION

The invention provides techniques for predicting the direction of a branch (taken or not taken) with relatively high accuracy and less on-chip area. The invention combines two types of predictors, a saturating counter branch predictor and a local branch history predictor, to provide an accurate prediction of the direction of a branch, based upon an address. The local history predictor has a local history table that includes an array of branch histories. If the local history table has a hit for the address, then its matching branch history is used to derive the final prediction. If the address results in a miss, then the output of the saturating counter branch predictor is used as the final prediction.

In a particular embodiment of the invention, the history field of a given entry in the local history table is updated with the outcome of an executed branch only if the local history predictor had yielded a correct prediction for the branch and the saturating counter predictor did not. In addition, a replacement field for a matching entry in the local history table is updated, only if the saturating counter prediction was incorrect. Such a scheme for populating the local history table provides for a more efficient utilization of the structure. There is a beneficial trade-off of area and performance for a certain set of applications. In particular, the predictor described provides a reasonable prediction for a large number of branches, using the saturating counter, and a more accurate prediction for a smaller number of branches, using the local branch history table. The accuracy of the local branch history table is not as high as a dynamically maintained local history table. However, the area not used in the dynamic table is used for the saturating counter, yielding a better overall predictor for programs with a large number of branches. In certain embodiments of the invention, the final prediction accuracy is comparable to the Yeh-Patt methodology discussed in the background,

while using less on-chip area. This provides the advantage that a greater number of branches may be tracked than using the conventional branch prediction methodologies, without increasing the on-chip area used by the branch direction predictor.

Fig. 1 illustrates a block diagram of branch direction prediction logic 100 according to an embodiment of the invention. A saturating counter branch prediction (SCBP) logic 104 and local branch history prediction (LBHP) logic 108 are provided on-chip in a processor. The SCBP 104 has an input that is coupled to receive an index value derived from an address. A first taken/not-taken prediction is provided at the output of the SCBP 104 responsive to the address. Similarly, the LBHP has an input coupled to receive an index value derived from the address. The LBHP 108 is capable of providing a second taken/not-taken prediction at an output responsive to the address resulting in a hit. A hit/miss indication is also provided by the LBHP 108 for the address. A multiplexer 112 has its inputs coupled to the outputs of the SCBP 104 and LBHP 108. In this embodiment of the invention, the multiplexer 112 has two single-line inputs one from each predictor logic, and one single-line output that provides the final taken/not-taken prediction. A select input of the multiplexer, in this case being a single line, is coupled to receive the hit/miss indication from the LBHP 108. The hit/miss indication thus selects either (1) the second prediction if there is a hit or (2) the first prediction if there is a miss.

In the particular embodiment of the branch prediction logic 100 shown in **Fig. 1**, the index values that are input to the SCBP 104 and LBHP 108 are obtained from address hash logic 116 which is coupled to an instruction pointer (IP) generator (not shown in **Fig. 1**). The address hash logic 116 provides a number of index values to the SCBP and LBHP logic based upon an input address received from the IP generator. The address hash logic 116 is only one example of what is in general any encoding or

compression scheme that helps make more efficient use of the relatively large number of bits in the address space of modern pipelined processors. For instance, if the address space is 64 bits wide, then the use of an encoding or compression scheme such as the address hash logic 116 generally allows a many-to-one mapping of several address values to a single index value. This, of course, means that each index value may represent several branch instructions. Such aliasing of the prediction mechanism may be tolerated as otherwise a prohibitively large local history table may be needed to separately track any branch instructions located at a given address value.

In a particular embodiment of the invention, the SCBP 104 includes an array of 2-bit predictors, one predictor for each index value. **Fig. 2** illustrates the state diagram of a 2-bit predictor. The predictor has four states, defined by two bits in a counter. The counter transitions from one state to another in response to a taken (T) or not-taken (N) outcome resulting from the execution of one or more branch instructions that are assigned to the index value of the predictor. The 2-bit predictor will always provide a prediction as to the direction of a branch, where if the counter is in states 01 or 00 the branch is predicted as N, while in states 10 and 11 the prediction is T. Although a 2-bit predictor is shown in the SCBP 104 of **Fig. 1**, in general saturating counters having greater than two bits may be used in the SCBP 104, although the benefits gained from using a greater number of bits in the counter may not outweigh the increased complexity and on chip area required by the resulting logic.

The LBHP 108 shown in **Fig. 1** includes a number of local branch history tables 120, where "local" refers to the accumulation of history (taken or not-taken) in each entry, that is specific to one or more branch instructions referenced by the index value of that entry. Each table entry has a tag field 128 and a history field 124, in addition to others not shown. The history field 124 contains a series of taken or not-taken outcomes

of one or more previously executed branch instructions that are associated with a unique tag value in the corresponding tag field 128 and an index value that is shared by all of the tables. The branch instructions may have been in the current program being executed, or they may have been part of a previously executed routine. For N local history tables, each index value looks up N tag-history entries where each entry corresponds to at least one branch instruction. This means that the configuration of **Fig. 1** can support, for each index value, separate histories for N distinct branch instructions. In a particular embodiment of the invention, all of these N branch instructions have the same lower (least significant) bits in their address values. See **Fig. 3** momentarily for an example of a mapping of these lower bits into the same index value.

The tables 120 are designed so that the index provided by the hash logic 116 preferably always matches that of an entry in each table 120. The tag value and the history value of the matching entry from each table 120 are provided to tag compare logic 132. The tags are then compared to a tag value derived from the address, by address hash logic 116. If one of the tags received from the tables 120 matches that derived from the address, then a "hit" is declared signifying that one of the tables 120 contains a taken/not-taken history of one or more branch instructions pointed to by the address. If a "miss" is declared, then the instructions pointed to by the address have no branch history within the tables 120. This hit or miss indication is used to select either the saturating counter prediction or the local history prediction to be the final prediction of the branch direction prediction logic 100 for the current address.

The history field corresponding to the matching tag field is selected by the tag compare logic 132 using a history multiplexer 136 and provided to combinational logic predictor 140. The combinational logic predictor 140 implements a decision function

whose output is either a taken or not-taken prediction based on the history value that has been provided to it. To help keep the on-chip area taken by the branch prediction logic 100 to a minimum, the combinational logic predictor 140 may have no memory, meaning that it does not have a counter or other state machine, and may simply be a combination of logic gates that are predetermined at the time the processor is built to generate a prediction based upon the taken/not-taken history that is provided to it.

The entries in the tables 120 of the LBHP 108 may be filled and updated while the processor is executing a test program or the actual program for which predictions are being made by the branch prediction logic 100. Whenever the processor is to execute a new program, the local history tables 120 may be wiped clean and refilled with new tag and history field values that are better suited to the new program, while the predictors in the SCBP 104 remain unchanged.

A new entry to the table 120 may be added when the prediction from SCBP 104 is incorrect. This procedure is controlled by entry replace logic 144 seen in **Fig. 1** which receives the actual branch direction of an executed branch from later stages of a pipeline (see **Fig. 4** discussed below.) A least recently used (LRU) algorithm may be employed to determine which is the existing entry to be replaced, although the invention need not be limited to any particular replacement algorithm.

The history field of an existing entry is updated with a new direction outcome of an executed branch. The replacement field for this entry is updated if the prediction by the SCBP 104 was incorrect. If the prediction was correct, then the replacement field is not updated which indicates the entry was not used. Such a functionality is implemented by history update logic 146. This gives a better utilization of the local history tables 120 because in this way the tables 120 are used only for compensating any mispredictions generated by the SCBP 104. If the predictions by the SCBP 104 remain

accurate, then the replacement fields of the LBHP 108 are not updated, thus allowing other branches to occupy the LBHP, which in turn means more efficient use of the on-chip area taken by the LBHP 108.

Fig. 3 illustrates using an example of the relationship between an address value and one or more instructions to which the address value points. It should be noted that the illustration is just one implementation of the hashing function used to encode bits in the address. In general, the encoded bits may come from anywhere in the address bits, not just the ones depicted in the figure. As was mentioned earlier, the address space of the pipelined processor may be relatively wide such that a large number of bits are used to derive the index value as well as the tag value. The tag concept is useful here because it allows a single branch instruction that may be part of multiple instructions within a cache line pointed to by the address to be extracted and uniquely identified by a unique tag. In general, tags provide a mechanism for uniquely identifying whether or not there is a branch at the address. If there are additional branch instructions within the same cache line, then these additional branch instructions may be assigned different tag values or additional offset values, yet all of these branch instructions in the same cache line will have the same index value. This is also a situation in which the address value may be hashed to derive the tag and index values that are fed to the SCBP and the LBHP logic (see **Fig. 1** momentarily). This is only one of several techniques that may be used to index into the SCBP and LBHP logic. As an alternative to using an encoding scheme to generate the index and the tag values, bits in the address value may be directly applied to index the local history tables 120 or the saturating counter predictor array in the SCBP logic. In addition, although in **Fig. 1** the address hash logic provides separate index values to the SCBP 104 and the LBHP 108, it may be possible to have only a common set of index values that are used by both SCBP 104 and the LBHP 108.

Turning now to **Fig. 4**, a block diagram of a pipelined processor that includes the branch prediction logic 100 is shown. In this embodiment of the invention, the pipeline has five stages although the invention is not limited to any particular number of stages or types of stages in a pipeline. The branch prediction logic 100 receives an address value from an IP generator 420 and immediately thereafter provides a taken/not-taken prediction. This taken/not-taken prediction may become available as soon as the address value is fed to the first stage of the pipeline, namely the instruction fetch stage 432. In the instruction fetch stage 432, one or more instructions at the address received from the IP generator 420 (the address for which a branch prediction was just made) are fetched from memory (not shown). It may be that one or none of these instructions that have been fetched is a branch instruction. The determination as to whether or not any of these fetched instructions is a branch, whether the branch is taken or not-taken, and the identity of the branch target address will not be available until the instructions have propagated through the later stages in the pipeline.

The taken/not-taken prediction is provided to IP control logic 436 which then uses this information to update the address provided by the IP generator 420. If T (taken) is predicted, then a target address determined by the decode stage 440 of the pipeline is loaded into the IP generator 420, so that the next instruction to be fetched for the pipeline will be from the target address.

The decode stage 440 of the pipeline is responsible for decoding the instruction which has been fetched from the current address. The instruction set of certain pipelined processors allows the target address of a branch instruction to be determined by the decode stage 440, without having to wait for the instruction to propagate through later stages of the pipeline. In the processor shown in **Fig. 4**, these later stages include register read 444 responsible for reading the contents of the registers that have

been specified by the instruction, and execute stage 448 in which the instructions are actually executed to yield results, and finally a writeback stage 452 in which the result is written to cache memory. In many instances, the outcome of a branch instruction, including its direction (whether taken or not) and the branch target address, become available at the output of the execute stage 448. This information is fed back to the branch direction predictor logic 100 to update the local history tables (see **Fig. 1** momentarily) and to the IP generator 420.

In the pipeline shown in **Fig. 4**, the direction prediction at the output of branch prediction logic 100 is available when the instruction pointed to by the address has been fetched and is provided to the decode stage 440. The prediction should be available no later than the point in time at which the target address has been determined by the decode stage 440, so that the IP generator 420 can be properly instructed, i.e. whether to change the address value by a predetermined increment or change it to the target address.

The branch prediction technique described here advantageously helps reduce the misdirect penalty by identifying non-branches, which are predicted taken by the saturation counter, early in the pipe. The decode stage 444 may determine whether the instruction which was predicted taken is actually a branch. If it is not, the instructions in the earlier states are removed, the instruction pointer is reset to the address following the non-branch which was misdirected, and the IP control block 436 accepts the prediction from branch direction prediction 100. Note that this mechanism is not necessary for proper functionality, but its presence increases performance and supports the performance/area argument mentioned earlier.

To summarize, various embodiments of the invention have been described that are directed to improved branch direction prediction methodologies implemented in

pipelined processors. The invention uses less on-chip area than other hardware-based local history predictors, while maintaining a comparable prediction accuracy. This allows the invention to track and predict a greater number of branches for the same area as a conventional predictor.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method comprising:

providing a first taken/not-taken prediction responsive to an address using a saturating counter branch predictor;

providing (1) a second taken/not-taken prediction responsive to the address resulting in a hit in a local branch history table, and (2) a hit/miss indication for the address; and

selecting for the address one of (1) the second prediction if the indication is a hit, and (2) the first prediction if the indication is a miss.

2. The method of claim 1 further comprising:

hashing the address prior to indexing at least one of the saturating counter branch predictor and the local branch history table.

3. The method of claim 1 further comprising:

updating a replacement field for a matching entry in the local branch history table only if the first prediction is incorrect, indicating that the entry is used to make a prediction.

4. The method of claim 1 further comprising:

fetching at least one instruction at the address; and

decoding the at least one instruction, wherein at least one of the first and second predictions is available when the at least one instruction is being decoded.

5. The method of claim 4 wherein the at least one instruction is a branch, the method further comprising:

determining a target address of the branch; and

loading an IP generator with the target address if at least one of the first and second predictions indicates that the branch is to be taken.

6. A processor comprising:

an instruction pointer (IP) generator capable of providing an address;

saturating counter branch prediction (SCBP) logic having an input coupled to the IP generator and capable of providing a first taken/not-taken prediction at an output responsive to the address;

local branch history prediction (LBHP) logic having an input coupled to the IP generator and capable of providing (1) a second taken/not-taken prediction at an output responsive to the address resulting in a hit, and (2) a hit/miss indication for the address; and

a multiplexer having an input coupled to the outputs of the SCBP and LBHP logic and a select input coupled to receive the hit/miss indication and in response provide (1) the second prediction if there is a hit and (2) the first prediction if there is a miss.

7. The processor of claim 6 further comprising:

address hash logic coupled between the IP generator and the inputs of the SCBP and LBHP logic to provide a plurality of index values to at least one of the SCBP and LBHP logic.

8. The processor of claim 6 wherein the SCBP logic includes a bimodal predictor.

9. The processor of claim 6 wherein the LBHP logic includes a plurality of local branch history tables each to provide a tag and a taken/not-taken history associated with the tag in response to a hit, compare logic coupled to each of the plurality of tables to determine the hit/miss indication, history multiplexer coupled to each of the plurality of tables to provide the history for the hit, and combinational logic coupled to an output of the history multiplexer to provide the second taken/not-taken prediction.

10. The processor of claim 6 wherein the LBHP logic includes at least one local branch history table to provide a tag and a taken/not-taken history in response to a hit, the processor further comprising:

entry replacement logic to update a replacement field for a matching entry in the at least one table only if the first prediction is incorrect.

11. The processor of claim 6 further comprising:

an instruction fetch stage of a pipeline; and

an instruction decode stage of the pipeline, and wherein the prediction at the output of the multiplexer is available when the address is being processed by an instruction decode stage of a pipeline.

12. The processor of claim 11 wherein the decode stage is capable of determining a target address of a branch instruction located at the address, the processor further comprising:

control logic coupled to load the IP generator with the branch target address if an output of the multiplexer indicates, for the address, that a branch is predicted to be taken.

13. The processor of claim 6 wherein the address points to a cache line having a plurality of instructions.

14. An apparatus comprising:

means for providing an address of at least one instruction;

means for providing a first taken/not-taken branch prediction based upon the current state of a state machine and responsive to the address;

local branch history prediction (LBHP) logic having an input coupled to the address providing means and capable of providing (1) a second taken/not-taken prediction at an output responsive to the address resulting in a hit, and (2) a hit/miss indication for the address; and

a multiplexer having an input coupled to the outputs of the first prediction means and the LBHP logic and a select input coupled to receive the hit/miss indication and in response provide (1) the second prediction if there is a hit and (2) the first prediction if there is a miss.

15. The apparatus of claim 14 further comprising:

means for encoding the address to provide a plurality of index values to at least one of the first prediction means and the LBHP logic.

16. The apparatus of claim 14 wherein the LBHP logic includes a plurality of local branch history prediction tables each to provide a tag and a taken/not-taken history associated with the tag in response to a hit, compare logic coupled to each of the plurality of tables to determine the hit/miss indication, history multiplexer coupled to each of the plurality of tables to provide the history for the hit, and combinational logic coupled to an output of the history multiplexer to provide the second taken/not-taken prediction.

17. The apparatus of claim 14 wherein the LBHP logic includes at least one local branch history prediction table to provide a tag and a taken/not-taken history in response to a hit, the processor further comprising:

means for updating a replacement field for a matching entry in the at least one table only if the first prediction is incorrect.

18. The apparatus of claim 14 further comprising:

means for fetching at least one instruction at the address; and

means for decoding the at least one instruction, wherein at least one of the first and second predictions is available when the at least one instruction is being decoded.

19. The apparatus of claim 18 wherein the at least one instruction is a branch, the apparatus further comprising:

means for determining a target address of the branch; and

means for fetching at least one instruction at the target address if at least one of the first and second predictions indicates that the branch is to be taken.

ABSTRACT

An embodiment of the invention is directed to a dynamic branch prediction method in which a first taken/not-taken prediction is provided responsive to an address using a saturating counter branch predictor. A second taken/not-taken prediction responsive to the address resulting in a hit in a local branch history table is provided. In addition, a hit/miss indication for the address is provided. The second prediction is selected for the address if the indication is a hit, and the first prediction is selected if the indication is a miss.

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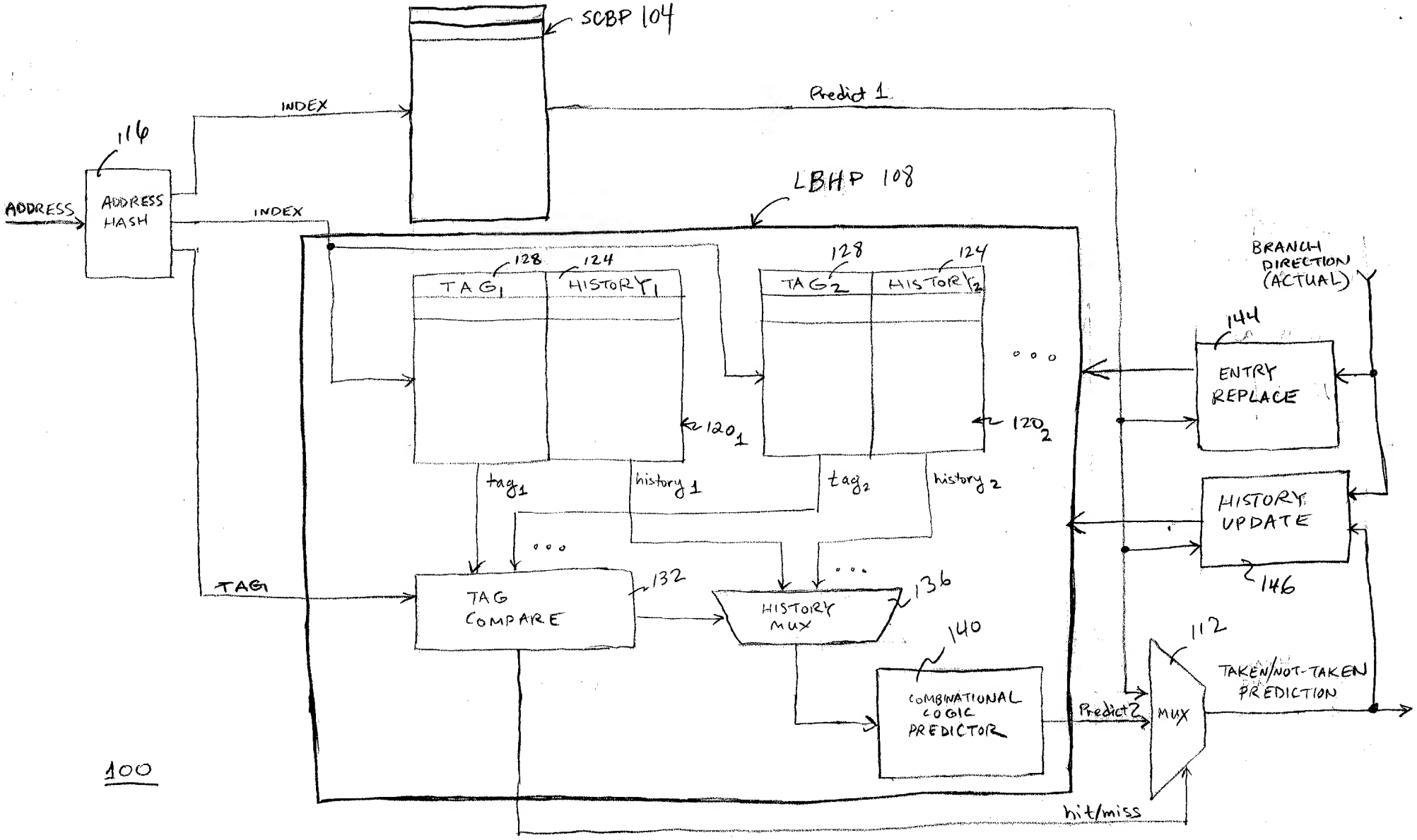

Fig. 1

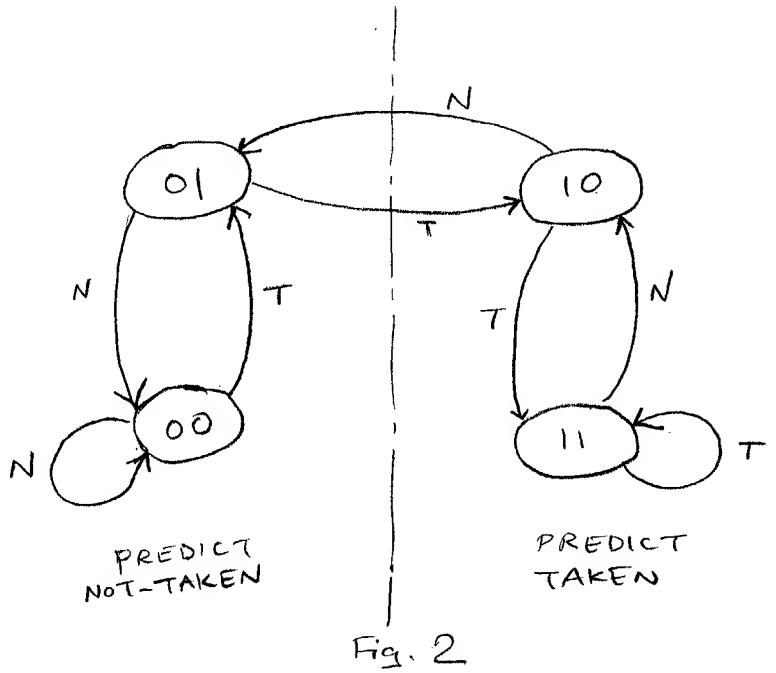

Fig. 2

042390.P5567

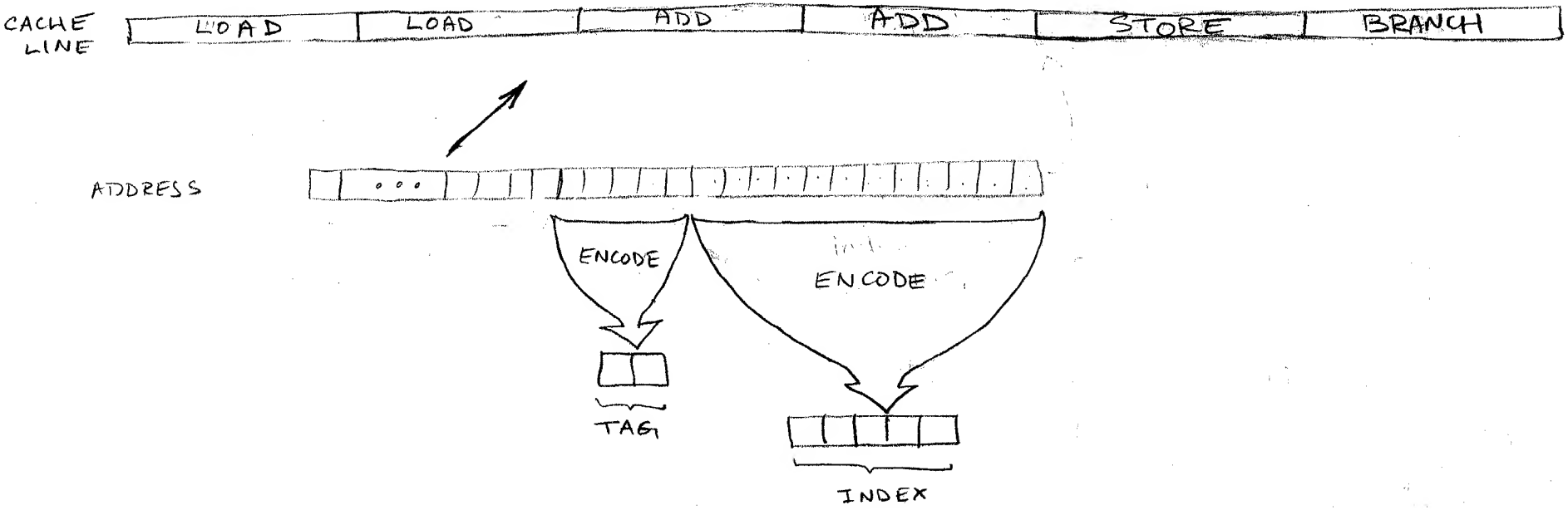

Fig. 3

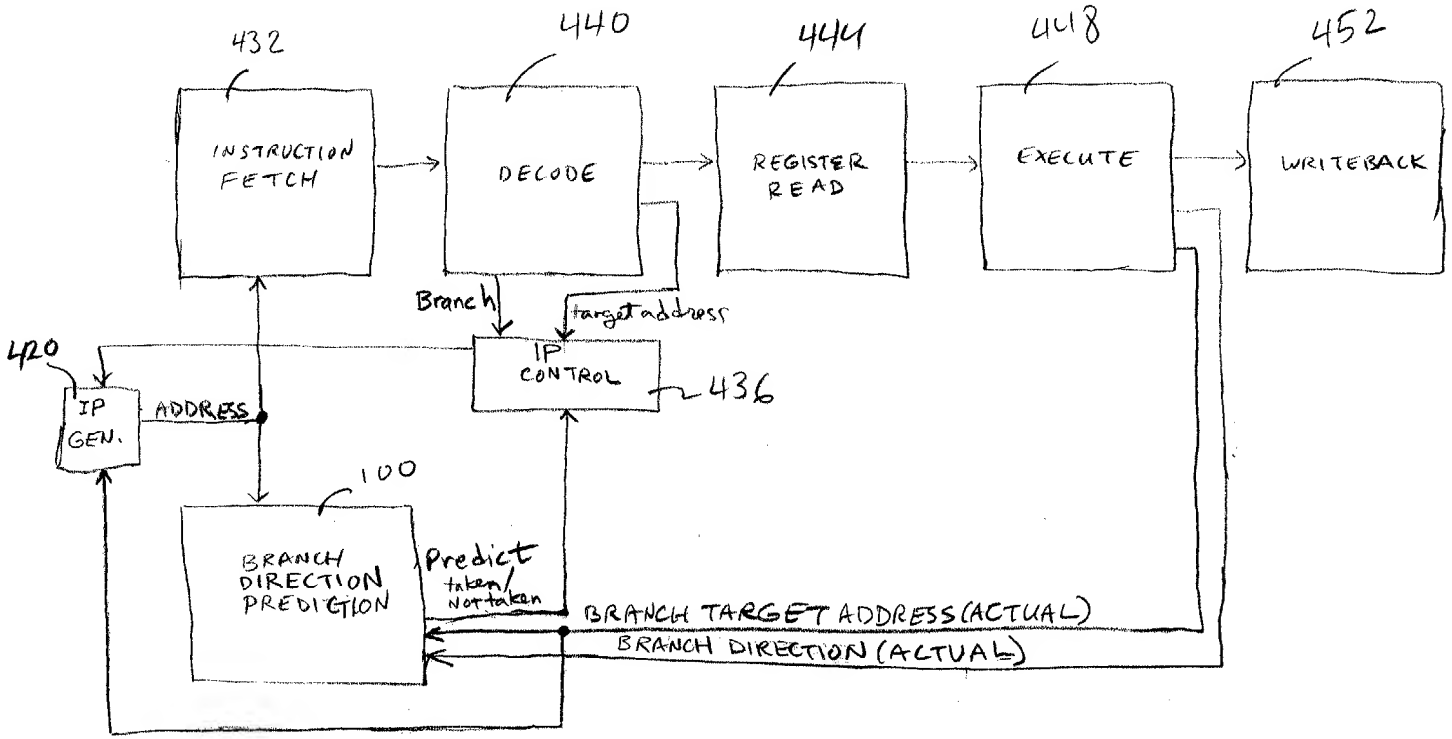
432
440
444
448
452
INSTRUCTION FETCH
DECODE
REGISTER READ
EXECUTE
WRITEBACK
Branch
target address
420
IP CONTROL
436
IP GEN.
ADDRESS
100
BRANCH DIRECTION PREDICTION
Predict taken/Not taken
BRANCH TARGET ADDRESS (ACTUAL)
BRANCH DIRECTION (ACTUAL)

Fig. 4

Attorney's Docket No.: 042390.P5567

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

BRANCH PREDICTOR WITH SATURATING COUNTER AND LOCAL BRANCH HISTORY TABLE

the specification of which

[X] is attached hereto.
[ ] was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, a firm including: William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. 42,261; Amy M. Armstrong, Reg. No. 42,265; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602: Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. 44,587; Thomas M. Coester, Reg. No. 39,637; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. 41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Eric T. King, Reg. No. 44,188; Erica W. Kuo, Reg. No. 42,775; Michael J. Mallie, Reg. No. 36,591; Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. No. 42,004; Chun M. Ng, Reg. No. 36878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Kimberley G. Nobles, Reg. No. 38,255; Lisa A. Norris, Reg. No. 44,976; Daniel E. Ovanezian, Reg. No. 41,236; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. No. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey S. Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. 45,241; Steven D. Yates, Reg. No. 42,242; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Andrew C. Chen, Reg. No. 43,544; Justin M. Dillon, Reg. No. 42,486; Paramita Ghosh, Reg. No. 42,806; Sang Hui Kim, Reg. No. 40,450; and John F. Travis, Reg. No. 43,203; my patent agents, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Peter Lam, Reg. No. P44,855; Thomas Raleigh Lane, Reg. No. 42,781; Gene I. Su, Reg. No. 45,140; and Calvin E. Wells, Reg. No. P43,256; my patent agents, of INTEL

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(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor (given name, family name) **Vincent E. Hummel**

Inventor's Signature Vincent E Hummel Date 3/27/00

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